REMARKS

Applicant respectfully requests reconsideration of this application as amended. Claims 2, 5, 6, 8, 13, 16-18, 26, 29, 31, and 32 are canceled. Claims 33-49 are added. Claims 1, 3, 4, 7, 9-12, 14, 15, 19 – 25, 27, 28, 30, and 33-49 are currently pending in this application.

*Claim Rejections - 35 U.S.C. §102(b)*

Claims 1, 3, 7, 9-12, 14, 19-25, 27, and 30 have been rejected under 35 U.S.C. §102(b) as being anticipated by Reisman et al. (U.S. Patent No. 4,891,329).

*Claim Rejections - 35 U.S.C. §103(a)*

Claims 4, 15, and 28 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Reisman in view of admitted prior art.

*Response to 35 U.S.C. §102(e) rejections*

With regard to the rejection of claims 1, 3, 7, 9-12, 14, 19-25, 27, and 30 under 35 U.S.C. §102(b) as being anticipated by Reisman, applicant has amended claims 1, 12, and 22 to overcome the examiner's rejection.

Specifically, applicant has added two limitations in these claims of "a second semiconductor substrate", and "bonding the first substrate directly to the second substrate".

Applicant submits that the added limitation of "a second semiconductor substrate" is supported in at least paragraph [0021], lines 10; and paragraph [0028], line 1. The added limitation of "bonding the first substrate directly to the second substrate" is supported by Fig. 1E, and paragraph [0029], lines 3-4.

Applicant submits that the present invention cannot be anticipated by Reisman because Reisman does not discloses a process of the present invention, namely bonding the insulator layer of the first substrate directly to the second semiconductor substrate.

Applicant submits that Reisman specifies that the bonding of the two substrates occurs at an insulator-insulator interface, with various exemplary insulator-insulator interface bonding techniques:

> *Then, insulating layer 30 is bonded to insulating layer 50 as shown at B. Typically, this is accomplished by thermally bonding insulating layers 30 and 50 together face-to-face to form a unified structure. Exemplary bonding techniques are disclosed in an article by Lasky entitled "Wafer Bonding For Silicon-On-Insulator Technologies" published in Applied Physics Letters, Vol. 48, No. 1, Jan. 6, 1986, and in an article by Frye et al entitled "A Field-Assisted Bonding Process For Silicon Dielectric Isolation" published in Journal of the Electrochemical Society, Vol. 133, No. 8, August 1986, the disclosures of which are hereby incorporated herein by reference.* (Col. 3, lines 53-65).

Applicant submits that the bonding process is different with different interfaces, as evidenced by the discussions of the two references cited by Reisman, specifically disclosing a bonding process for two insulator surfaces without any mentioning of other interfaces. Thus applicant submits that the bonding between an insulator surface and a semiconductor surface is distinct from bonding between two insulator surfaces, and that one bonding process cannot be anticipated from the other.

In sum, applicant submits that the present invention cannot be anticipated by Reisman because Reisman fails to disclose an operation of the present invention, namely bonding directly the insulator layer of the first substrate to the second semiconductor substrate. Further, applicant submits that the bonding between insulator and semiconductor surfaces is distinct from the bonding between two insulator surfaces, thus the present invention is not rendered obvious from the teaching of Reisman, who discloses bonding process for two insulator surfaces.

With regard to the dependent claim 3, 14, and 27, applicant submits that Reisman only discloses a etch process, such as wet chemistry, plasma or reactive ion etching (Col. 4, lines 66-68). Applicant submits that Reisman is silent with respect to a grind back process or an ion exfoliation process. Thus applicant submits that these claims are not anticipated by Reisman.

With regard to the dependent claim 7, and 30, applicant submits that Reisman only discloses a etch process, such as wet chemistry, plasma or reactive ion etching (Col. 4, lines 66-68). Applicant submits that Reisman is silent with respect to a cleaving off process to remove the first substrate after bonding. Thus applicant submits that these claims are not anticipated by Reisman.

With respect to the dependent claims, applicant submits that these claims are dependent claims, thus should be allowable, at least for the reason stated above with respect to the independent claims 1, 12 and 22.

*Response to 35 U.S.C. §103(a) rejections*

With respect to the rejection of claims 4, 15, and 28 under 35 U.S.C. §103(a) as being unpatentable over Reisman in view of admitted prior art, applicant submits that the additional operation of "polishing the surface of the first dielectric film prior to the bonding" is novel and not obvious over Reisman in view of admitted prior art.

Applicant submits that the teaching of applicant, as quoted by the Examiner, constitutes an embodiment of the present invention, and not an admitted prior art:

> *In one embodiment, the dielectric layer 106 is polished using a conventional method such as chemical mechanical polishing (CMP) to remove some of the dielectric layer 106.* (Paragraph [0027], last sentence).

Applicant submits that the admitted prior art in this teaching is that CMP is a conventional method of polishing. The polishing of the dielectric layer prior to bonding to the semiconductor substrate is disclosed by the applicant as an embodiment of the invention, and not admitted prior art.

Thus applicant submits that Reisman is silent with respect to a polishing process of the insulator layer of the first substrate before the bonding process. Applicant submits that there is no motivation to combine the prior art knowledge that CMP is a conventional method of polishing with Reisman's teaching of bonding two insulator surfaces. Thus

applicant submits that the combination of Reisman and the admitted prior art does not render obvious the present invention polishing an insulator surface before the bonding process.

Furthermore, the polishing process is motivated by applicant's observation of the roughness of the deposited germanium layer. Since polishing the germanium surface is time consuming (Paragraph [0006], last sentence), the present invention discloses the novel process of polishing the insulator layer on top of the germanium layer before the bonding process. Thus applicant submits that the polishing operation is novel and cannot be rendered obvious from Reisman.

Applicant further adds claims 33-49 to independently claim the process of polishing the dielectric layer prior to bonding the second substrate to the dielectric layer of the first substrate.

In conclusion, applicants respectfully submit that in view of the amendments and arguments set forth herein, the applicable rejections have been overcome.

Please charge any shortages and credit any overcharges to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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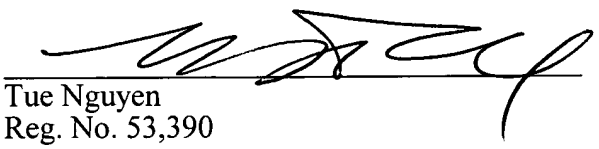

Tue Nguyen
Reg. No. 53,390

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8300